REMARKS

I. REAL PARTY IN INTEREST

The present Application was assigned to Altera Corporation, a Delaware corporation, as indicated by an assignment from the inventors recorded on February 9, 2004 in the Assignment Records of the United States Patent and Trademark Office at Reel 014985, Frame 0023.

II. RELATED APPEALS AND INTERFERENCES

Appellants, the undersigned Attorney, and Assignee are not aware of any related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal of this application.

III. STATUS OF CLAIMS

Claims 1-61 remain in the present application.

Claim 59 is rejected under 35 U.S.C. §101 as being directed to non-statutory matter.

Claim 59 is rejected under 35 U.S.C. §112, first paragraph as being a "single step/means" claim.

Claims 59-60 are rejected under 35 U.S.C. §112, second paragraph as being indefinite.

Claims 1-61 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,973,632 ("Brahme").

Claims 59-61 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent 5,649,167 ("Chen").

IV. STATUS OF AMENDMENTS

This response after final is filed on November 15, 2006 in response to an Office Action mailed August 15, 2006. No amendments to the claims have been made subsequent to the Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

With respect to independent Claim 1 a method for designing a system includes determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy short-path and long-path timing constraints for the path (See Figure 4, 404, Figures 5-7, and pages 13, lines 4-14, and page 13, line 18 to page 18, line 22, and page 19, line 23 to page 20, line 4). Routing resources are selected for the connections in response to the minimum and maximum delay budgets (See Figure 7 and page 18, line 23 to page 21, line 21).

With respect to independent Claim 33 a machine-readable medium is disclosed (See page 28, lines 8-15). The machine-readable medium having stored thereon sequences of instructions, the sequences of instructions including instructions which, when executed by a processor, causes the processor to perform determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy short-path and long-path timing constraints for the path (See Figure 4, 404, Figures 5-7, and pages 13, lines 4-14, and page 13, line 18 to page 18, line 22, and page 19, line 23 to page 20, line 4). Routing resources are selected for the connections in response to the minimum and maximum delay budgets (See Figure 7 and page 18, line 23 to page 21, line 21).

With respect to independent Claim 48, a system designer includes a slack allocator unit that generates minimum and maximum delay budgets for connections along a path from long-path and short-path timing constraints for the path provided by a user (See Figure 2, 240, and page 9, line 18 to page 10, line 2). The system designer includes a routing unit that selects

routing resources in a system to route the connections in response to the minimum and maximum delay budgets (See Figure 2, 230, and page 10 lines 3-14).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Was Claim 59 properly rejected under 35 U.S.C. §101 as being directed to non-statutory matter.

2. Was Claim 59 properly rejected under 35 U.S.C. §112, first paragraph as being a "single step/means" claim.

3. Were Claims 59-60 properly rejected under 35 U.S.C. §112, second paragraph as being indefinite.

4. Were Claims 1-58 properly rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,973,632 ("Brahme").

5. Were Claims 59-61 properly rejected under 35 U.S.C. §102(b) and §102(e) as being unpatentable over Brahme and U.S. Patent 5,649,167 ("Chen").

VII. ARGUMENT 1

Claim 59 was improperly rejected under 35 U.S.C. §101 as being directed to non-statutory matter.

Claims 59-61 is rejected under 35 U.S.C. §101 as being directed to non-statutory matter. Specifically, the Office Action mailed 8/15/2006 states

> The act of the claimed expresses an abstract idea of selecting routing resources to increase delay for connection without specifies any data, functional, or practical application is non-statutory, see MPEP 2106 [R-3].

(8/15/2006 Office Action, p. 2).

Claims 59-61 include the limitation of "selecting routing resources". Applicants submit that the "routing resources" are physical objects. The Federal Circuit Court of Appeals has ruled that the manipulation of data representing physical objects or activities, where the data comprises signals corresponding to physical objects or activities external to the computer system and the process causes a physical transformation of the signals which are intangible representation of the physical objects or activities, constitutes a statutory process (see In re Schrader 22 F.3d 290, 294 (Fed. Cir. 1994) and Arrhythmia Research Tech. v. Corazonix Corp, 958 F.2d 1053, 1058-1059 (Fed. Cir. 1992) and also MPEP 2106, p. 2100-16 (Rev. 3 August 2005) which states that the subject matter constitutes a safe harbor for being statutory).

Applicants submit that in view of the state of the law summarized above, the rejections to claims 59-61 have been overcome.

VIII. ARGUMENT 2

Claim 59 was improperly rejected under 35 U.S.C. §112, first paragraph as being a "single step/means" claim.

Claims 59 is rejected under 35 U.S.C. §112, first paragraph as being a "single step/means" claim. The Office Action mailed 8/15/2006 cites MPEP 2164.08(a).

Applicants submit that MPEP 2164.08(a) applies only to "Single Means Claim". Applicants submit that 35 U.S.C. §112, first paragraph has been mis-applied to claim 59 because claim 59 does not include any such "means" language or equivalent. To the contrary, claim 59 includes the language

> A method for designing a system, comprising:
> selecting routing resources to increase delay for connections in response to path-level hold time requirements.

(Claim 59).

Thus, claim 59 clearly includes an act ("selecting routing resources") and is not drafted in "means-plus-function" format. Applicants respectfully submits that 1) there is no general prohibition against a single step or single element claim, and 2) claims 59-61 do not include "means" language or equivalents and thus a 35 U.S.C. §112, first paragraph is improper. Furthermore, applicants note that other recently issued patents from the Patent Office have included single step claims. Applicants refer the Examiner to claim 8 of U.S. Pat. No. 7,124,271 issued 10/17/2006. Applicants respectfully requests the Examiner to reconcile the difference in the interpretation of 35 U.S.C. §112, first paragraph between the case of patent no. '271 and the present application.

Applicants submit that the rejections under 35 U.S.C. §112, first paragraph have been overcome.

IX. ARGUMENT 3

Claims 59-60 were improperly rejected under 35 U.S.C. §112, second paragraph as being indefinite.

Claims 59-60 are rejected under 35 U.S.C. §112, second paragraph as being indefinite. Specifically, the Office Action mailed 8/15/2006 states

> This claim recites the limitation "selecting routing resources to ... "is unclear and incomplete as to routing resources of/from what/where, and "hold time requirements" is unclear and incomplete as to hold time of/from/what/where. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

(8/15/2006 Office Action, pp. 2-3).

MPEP 2173.04, however, is clear in stating that

> Breadth of a claim is not to be equated with indefiniteness. In re Miller, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject mater embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the

> invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.

(MPEP 2173.04, p. 2100-213, Rev. 5, Aug. 2006) (Emphasis Added).

Applicants submit that "routing resources" and "path-level hold time requirements" are well known terminologies that are familiar to those skilled in the art. Furthermore, applicants submit that applicants are not claiming "of/from what/where" of the "routing resources" or "path-level hold time requirements".

Claims 59-60 are rejected under 35 U.S.C. §112, second paragraph as being indefinite.

The Office Action states that

> Claim 59-60 are rejected because "increase delay" and "minimum delay" are contradicting claimed limitations without clear justification, Thus, clear and indefinite.

(8/15/2006 Office Action. p. 2).

Applicants submit that the claim limitations of "to increase delay" and "determining a minimum delay budget" are ***NOT*** contradicting claim limitations. Applicants refer the Examiner to the specification for clarification and a better understanding of the claimed invention.

> A short-path timing constraint indicates that the delay from one end of the path to the other end must be no smaller than Y. The path-level timing constraints are translated into connection-level constraints (minimum and maximum delay budgets). Minimum and maximum delay budgets for each connection are determined which may be used to guide technology mapping, placement, and routing on a PLD such that performance goals are satisfied. A minimum delay budget indicates that the delay of the respective connection should be no smaller than X.

(Specification, p. 4) (Emphasis Added).

Applicants submit that "minimum delay budgets" are determined that allows for connections to satisfy path-level timing constraints (such as short-path timing constraints) so that appropriate routing resources that "increase delay" may be selected. Additional details as to how the "minimum delay budgets" are generated and which "routing resources" are selected are described in Figures 5-8 and its corresponding text.

Applicants submit that the rejection to claims 59-60 under 35 U.S.C. §112, second paragraph have been overcome.

X. ARGUMENT 4

Claims 1-58 were improperly rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,973,632 ("Brahme").

Claims 1-61 are grouped into the following groups.

Group I: Claims 1-58

The claims in Group I stand or fall together.

Group II: Claims 8-18, and 40-42

The claims in Group II stand or fall together.

Group III: Claims 20 and 44

The claims in Group III stand or fall together.

Group IV: Claims 21, 22, 45, 46

The claims in Group IV stand or fall together.

Group V: Claim 56

Group VI: Claim 57

Group VII: Claim 58

The Examiner has rejected claims 1-61 under 35 U.S.C. §102(e) as being anticipated by Brahme. In particular, the Examiner has stated that

> As to claims 1, and 33, Brahme et al. teach a method for designing a system, comprising: determining minimum and maximum delay budgets for connections by finding a set of connection delays that attempt to satisfy the short-path (see fig 9 element 931, and fig 10 element 1033) and long-path (see fig 9 element 933, and fig 10 element 1031) timing constraints for the path (see fig 3 Fig. 4, fig 5, fig 6-8, element 405-417, col 6 line 10 to col 8 line 11, and Especially, and fig 9-10 col 9 lines

> 19-53, and col 6 line 40 to col 7 line 3); and selecting routing resources for the connections in response to the minimum and maximum delay budgets (see fig 4-10 element 417 col. 2 line 14 to col 3 line 16, and col 6 line 60 to col. 7 lines 51).

(8/15/2006 Office Action, p. 3)

It is submitted that Brahme does not render claims 1-61, unpatentable under 35 U.S.C. §102(e).

Brahme includes a disclosure of methods and apparatuses to estimate delay for logic circuit optimization using back annotated placement and delay data. In one aspect, a method to design a logic circuit, the method includes: modifying a first path that is back annotated with first placement information and first delay information to generate a second path; and calculating a signal delay on the second path from second placement information for the second path, the first placement information and the first delay information (or, computing an adjustment to the first delay information from second placement information for the second path and the first placement information). In one example according to this aspect, the first placement information and the first delay information are back annotated from a timing analysis based on placing and routing at least the first path. An actual route is determined from the first placement information in calculating the signal delay (see Brahme Abstract).

It is submitted that Brahme does not teach or suggest determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy short-path and long-path timing constraints for the path, and selecting routing resources for the connections in response to the minimum and maximum delay budgets.

On the contrary, Brahme discloses techniques for reducing delay along a path and is concerned with only the maximum delay along a path where the delay may be too long and has to be reduced to meet a long-path timing constraint. Brahme does not

address the minimum delay along a path where the delay may be too short and has to be increased to meet short-path timing constraints. Brahme does not generate both minimum and maximum delay budgets to satisfy both long-path and short path timing constraints.

Brahme discloses changing a placement of a logic element for meeting timing requirements. If the slack on an output side of a flip flop 901 is worse than the slack on the input side of the path for the flip-flop 901 and the wire delay on the path 933 is too long, flip-flop 901 is moved toward load logic element 909 as shown by flip-flop 101 in Figure 10 (see Brahme col. 9 lines 19-48 and Figures 9 and 10). Brahme also discloses a technique of replicating a logic element for meeting timing requirements where to reduce the delay on the path from logic element 1103 to load logic element 1107, flip-flop 1103 may be replicated as flip flop 1203, as shown in Figure 12 (see Brahme col. 9, lines 54 to col. 10, line 2 and Figures 11 and 12). Other replication and restructuring techniques are also disclosed to reduce excessive delays (see Brahme col. 10, lines 15-29, and Figures 13 and 14). None of these techniques or methods involve determining both a minimum and maximum delay budget for connections along a path by finding a set of delays that satisfy both short-path and long-path timing constraints for the path.

In summary, Brahme fails to disclose 1) both short-path and long-path timing constraints, and 2) determining both minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy the short-path and long-path timing constraints.

In contrast, claim 1 states

> A method for designing a system, comprising:
> determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy short-path and long-path timing constraints for the path; and
> selecting routing resources for the connections in response to the minimum and maximum delay budgets.

(Claim 1) (Emphasis added).

Claims 33 and 48 include similar limitations. Given that claims 2-32, 52-58, depend from claim 1, claims 34-47 depend from claim 33, and claims 49-51 depend from claim 48, it is likewise submitted that claims 2-32, 34-47, and 49-58 are also patentable under 35 U.S.C. §102(e) over Brahme.

It is submitted that Brahme does not teach or suggest determining minimum and maximum delay budgets for the connections by allocating short-path and long-path slack.

The Examiner cites Figures 3-10, and Figures 15-16, column 7 line 13 to column 9, line 48 (specifically col. 8, lines 12-62) as evidence that Brahme teaches "determining minimum and maximum delay budgets for the connections comprises allocating short-path and long-path slack" (2/23/06 Office Action, p. 5). Applicants submit that the cited sections by the Examiner do not disclose the allocation of short-path or long-path slack to establish minimum and maximum delay budgets used for selecting routing resources. In fact, Applicants could not find any disclosure or mention of short-path and long-path slack in the entire Brahme reference. The Brahme reference discloses delay estimation used to guide timing optimization. Applicants respectfully request the Examiner to clarify how the cited text renders claim 8 unpatentable.

In contrast, claim 8 states

> The method of Claim 1, wherein determining minimum and maximum delay budgets for the connections comprises allocating short-path and long-path slack.

(Claim 8) (Emphasis added).

Claim 40 includes similar limitations. Given that claims 9-18 and claims 41-42 depend directly or indirectly on claims 8 and 40, it is likewise submitted that claims 9-18 and 41-42 are also patentable under 35 U.S.C. §102(e) over Brahme.

It is submitted that Brahme does not teach or suggest re-selecting routing resources for connections that are shorted.

The Examiner cites Figures 3-8, column 6, line 28 to column 7 line 50, and summary as evidence that Brahme teaches "wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises re-selecting the routing resources for connections that are shorted" (8/15/06 Office Action, p. 7). Applicants submit that the cited sections by the Examiner do not disclose re-selecting routing resources for connections that are shorted. In fact, Applicants could not find any disclosure or mention of shorted connections in the entire Brahme reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 20 unpatentable.

In contrast, claim 20 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises re-selecting the routing resources for connections that are shorted.

(Claim 20) (Emphasis added).

Claim 44 includes similar limitations.

It is submitted that Brahme does not teach or suggest either decreasing minimum delay budgets based on the number of routing iterations that have occurred or increasing maximum delay budgets based on the number of routing iterations that have occurred.

The Examiner cites Figures 2, and 3-8, column 2, lines 14-49, and column 7, line 13 to column 8, line 61 as evidence that Brahme teaches "decreasing minimum delay budgets based on the number of routing iterations that have occurred" and "increasing maximum delay budgets based on the number of routing iterations that have occurred" (8/15/06 Office Action, p. 7). Applicants submit that the cited sections by the Examiner

do not disclose decreasing minimum delay budgets based on the number of routing iterations that have occurred or increasing the maximum delay budgets based on the number of routing iterations that have occurred. In fact, applicants could not find any disclosure of mention of routing iteration in the entire Brahme reference. Applicants respectfully request the Examiner to clarify how the cited text render claims 21 and 22 unpatentable.

In contrast, claim 21 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises decreasing minimum delay budgets based on the number of routing iterations that have occurred.

(Claim 21) (Emphasis added).

Claim 45 includes similar limitations.

Claim 22 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises increasing maximum delay budgets based on the number of routing iterations that have occurred.

(Claim 22) (Emphasis added).

Claim 46 includes similar limitations.

It is submitted that Brahme also does not teach or suggest short-path timing constraints that comprises a hold time requirement.

The Examiner cites Figures 3-10, element 405-417, column 6, line 10 to column 8, line 11, column 9, line 19-53 as evidence that Brahme "teach wherein the short-path timing constraints comprises a hold time requirement" (8/15/2006 Office Action, p. 11). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a hold time requirement. In fact applicants could not find any disclosure or mention of hold time requirements in the entire Brahme reference.

Applicants respectfully request the Examiner to clarify how the cited text renders claim 56 unpatentable.

In contrast, claim 56 states

> The method of Claim 1, wherein the short-path timing constraints comprises a hold time requirement.

(Claim 56) (Emphasis Added).

It is submitted that Brahme also does not teach or suggest short-path timing constraints that comprises a minimum propagation delay.

The Examiner cites Figures 3-10 and 15-16, column 7, line 13 to column 9, line 53 as evidence that Brahme "teach wherein the short-path timing constraints comprises a minimum propagation delay" (8/15/2006 Office Action, p. 11). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a minimum propagation delay. In fact, applicants could not find any disclosure or mention of a minimum propagation delay in the entire Brahme reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 57 unpatentable.

In contrast, claim 57 states

> The method of Claim 1, wherein the short-path timing constraints comprises a minimum propagation delay.

(Claim 57) (Emphasis Added).

It is submitted that Brahme also does not teach or suggest short-path timing constraints that comprises a minimum clock-to-output requirement.

The Examiner again cites Figures 3-10 and 15-16, column 7, line 13 to column 9, line 53 as evidence that Brahme "teach wherein the short-path timing constraints comprises a minimum clock-to-output requirement" (8/15/2006 Office Action, p. 11). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a minimum clock-to-output requirement. In fact,

applicants could not find any disclosure or mention of a minimum clock-to-output requirement in the entire Brahme reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 58 unpatentable.

In contrast, claim 58 states

> The method of Claim 1, wherein the short-path timing constraints comprises a minimum clock-to-output requirement.

(Claim 58) (Emphasis Added).

XI. ARGUMENT 5

Claims 59-61 were improperly rejected under 35 U.S.C. §102(b) and §102(e) as being unpatentable over Brahme and U.S. Patent 5,649,167 ("Chen").

Group VIII include Claims 59-61.

The claims in Group VIII stand or fall together.

It is submitted that neither Brahme nor Chen teach or suggest selecting routing resources to increase delay for connections in response to path-level hold time requirements.

The Office Action mailed 8/15/2006 states that

> As to claim 59, Brahme et al. teach a method for designing a system, comprising: selecting routing resources to increase delay for connections in response to path-level hold time (see fig. 9, fig 10 element 901, 1001) requirements (see fig 3 Fig. 4, fig 5, fig 6-8, element 405-417, col 6 line 10 to col 8 line 11, and Especially, and fig 9-10 col 9 lines 19-53, and col 6 line 40 to col 7 line 3).
>
> . . .
>
> As to claim 59, Chen t al. teach a method for designing a system, comprising: selecting routing resources to increase delay for connections in response to path-level hold time requirements (see fig 12-14 col 1 line 49 to col 2 line 8, and 10 line 54 to col 12 line 42).

(8/15/2006 Office Action, pp. 11-12)

Brahme discloses techniques such as changing the placement of a logic element, replicating logic element, and restructuring a logic element in order reduce the delay of a signal along a path (see Brahme col. 9, line 19 through col. 11, line 64, and Figures 9-20). None of these techniques are used to increase delay for connections in response to path-level hold time requirements. In fact, no where in Brahme is path-level hold time requirements discussed. Applicants respectfully request the Examiner to clarify how the cited text renders claim 59 unpatentable.

Chen discloses a technique that partitions a logic design across multiple reprogrammable logic circuits. The partitioning is performed to repair hold time violations. Chen discloses constraining the design partitioning solutions to insert unclocked FPGAs on hold problematic paths (see Chen col. 2, line 32 to col. 3, line 11). Chen does not select routing resources to increase delay.

In contrast, claim 59 states

> A method for designing a system, comprising:
> selecting routing resources to increase delay for connections in response to path-level hold time requirements.

(Claim 59) (Emphasis Added).

Given that claims 60-61 depend from claim 59, it is likewise submitted that claims 60-61 are also patentable under 35 U.S.C. §102(e) over Brahme and §102(b) over Chen.

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-61 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: November 15, 2006

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of November, 2006.

Lawrence M. Cho